This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method of generating carry information during an arithmetic operation of a first input signal A and second input signal B, the method comprising:

generating a plurality of carry-create signals in response to logical combinations of corresponding first groups of bit pairings of the first and second input signals;

generating a plurality of carry-transmit signals in response to logical combinations of corresponding second groups of bit pairings of the first and second input signals, wherein the first groups of bit pairings are different from the second groups of bit ~~pairing~~ pairings; and

logically combining the carry-create and carry-transmit signals to create a number of accumulated carry-create signals that represent accumulated carry information at predetermined bit intervals,

wherein each carry-create signal is generated according to the logical expression $J[z \rightarrow x] = (Az \mid Bz) + (Ay \mid By) + (Ax \mid Bx)$, where $\mid$ is the logical AND operation and + is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals.

Claim 2 (canceled)

Claim 3 (original): The method of Claim 1, wherein each carry-transmit signal is generated according to the logic expression $T[z \rightarrow x] = (Az + Bz) \mid [(Ay + By) \mid (Ax + Bx) + (Ay \mid By)]$, where $\mid$ is the logical AND operation and + is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals.

Claim 4 (original): The method of Claim 1, wherein the logically combining step is implemented using carry look-ahead logic.

Claim 5 (original): The method of Claim 1, further comprising:

generating a number of carry translation signals in response to logical combinations of corresponding third groups of bit pairings of the first and second input signals;

generating a number of pairs of complementary pre-sum signals in response to a logical addition of the input signals;

logically combining the carry translation signals with corresponding pairs of complementary pre-sum signals to generate a number of pairs of complementary sum signals; and

selecting one from each pair of complementary sum signals in response to corresponding accumulated carry-create signals to generate a sum signal.

Claim 6 (original): The method of Claim 5, wherein each carry translation signal is generated according to the logical expression $CT[y \rightarrow x] = (Ay + By) \mid (Ax + Bx) + (Ay \mid By)$, where $\mid$ is the logical AND operation and + is the logical OR operation, and x and y represent consecutive bit positions of the input signals.

Claim 7 (original): The method of Claim 1, further comprising:

generating a number of carry translation signals in response to logical combinations of corresponding third groups of bit pairings of the first and second input signals;

logically combining each of the carry translation signals with a corresponding accumulated carry-create signal to generate a number of accumulated carry-generate signals;

generating a number of pairs of complementary sum signals in response to a logical addition of the input signals; and

selecting one from each pair of complementary sum signals in response to corresponding accumulated carry-create signals to generate a sum signal.

Claim 8 (currently amended): An adder for generating carry information during an arithmetic operation of a first input signal A and second input signal B, comprising:

means for generating a plurality of carry-create signals in response to corresponding first groups of bit pairings of the first and second input signals;

means for generating a plurality of carry-transmit signals in response to corresponding second groups of bit pairings of the first and second input signals, wherein the first groups of bit pairings are different from the second groups of bit pairings;

means for logically combining the carry-create and carry-transmit signals to create a number of accumulated carry-create signals that represent accumulated carry information at predetermined bit intervals,

wherein the means for generating the carry-transmit signal comprises a logic circuit configured to implement the logical expression $T[z \rightarrow x] = (Az + Bz) \mid [(Ay + By) \mid (Ax + Bx) + (Ay \mid By)]$, where $\mid$ is the logical AND operation and + is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals.

Claim 9 (original): The adder of Claim 8, wherein the means for generating the carry-create signal has a stack height of two.

Claim 10 (original): The adder of Claim 8, wherein the means for generating the carry-create signal comprises a logic circuit configured to implement the logical expression $J[z \rightarrow x] = (Az \mid Bz) + (Ay \mid By) + (Ax \mid Bx)$, where | is the logical AND operation and + is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals.

Claim 11 (original): The adder of Claim 8, wherein the means for generating the carry-transmit signal has a stack height of three.

Claim 12 (canceled)

Claim 13 (original): The adder of Claim 8, wherein the means for combining comprises carry look-ahead logic.

Claim 14 (original): The adder of Claim 8, further comprising:

means for generating a number of carry translation signals in response to logical combinations of corresponding third groups of bit pairings of the first and second input signals;

means for generating a number of pairs of complementary pre-sum signals in response to a logical addition of the input signals;

means for logically combining the carry translation signals with corresponding pairs of complementary pre-sum signals to generate a number of pairs of complementary sum signals; and

means for selecting one from each pair of complementary sum signals in response to corresponding accumulated carry-create signals to generate a sum signal.

Claim 15 (original): The adder of Claim 14, wherein the means for generating the carry translation signal comprises a logic circuit configured to implement the logical expression $CT[y \rightarrow x] = (Ay + By) \mid (Ax + Bx) + (Ay \mid By)$, where $\mid$ is the logical AND operation and + is the logical OR operation, and x and y represent consecutive bit positions of the input signals.

Claim 16 (original): The adder of Claim 8, further comprising:

means for generating a number of carry translation signals in response to logical combinations of corresponding third groups of bit pairings of the first and second input signals;

means for logically combining each of the carry translation signals with a corresponding accumulated carry-create signal to generate a number of accumulated carry-generate signals;

means for generating a number of pairs of complementary sum signals in response to a logical addition of the input signals; and

means for selecting one from each pair of complementary sum signals in response to corresponding accumulated carry-create signals to generate a sum signal.

Claim 17 (original): An adder for generating carry information during an arithmetic operation of a first input signal A and second input signal B, comprising:

a plurality of carry-create circuits, each for generating a carry-create signal J in response to corresponding bit pairings of the input signals according to the logical expression $J[z \rightarrow x] = (Az \mid Bz) + (Ay \mid By) + (Ax \mid Bx)$, where $\mid$ is the logical AND operation, + is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals;

a plurality of carry-transmit circuits, each for generating a carry-transmit signal T in response to corresponding bit pairings of the input signals according to the logical expression $T[z \rightarrow x] = (Az + Bz) \mid [(Ay + By) \mid (Ax + Bx) + (Ay \mid By)]$; and

carry look-ahead logic for logically combining the carry-create signals and the carry-transmit signals to generate a number of accumulated carry-create signals that represent accumulated carry information at predetermined bit intervals.

Claim 18 (original): The adder of Claim 17, further comprising:

a plurality of carry translation circuits, each for generating a carry translate signal CT in response to corresponding bit pairings of the input signals according to the logical expression $CT[y \rightarrow x] = (Ay + By) \mid (Ax + Bx) + (Ay \mid By)$.

Claim 19 (original): The adder of Claim 18, where the carry-translate circuit is incorporated within the carry-transmit circuit.

Claim 20 (original): The adder of Claim 18, further including a number of sum generators, each comprising:

a sum circuit for generating pairs of complementary pre-sum bits in response to logical additions of corresponding bits of the input-signals;

translation logic having inputs to receive the pairs of complementary pre-sum signals, an input to receive a corresponding carry-translation signal, and outputs to provide pairs of complementary sum bits; and

a multiplexer having inputs to receive the pairs of complementary sum bits, a select terminal to receive a corresponding accumulated carry-create signal, and an output to provide corresponding bits of a sum signal.

Claim 21 (original): The adder of Claim 20, wherein the translation logic translates pairs of complementary pre-sum bits into corresponding pairs of complementary sum bits.

Claim 22 (original): The adder of Claim 20, wherein each sum generator generates the sum bits S [5:3] according to the logical expression S [5:3] = J [2→0] | CT [2→1] | SUM1 [5: 3] + JB[2→0] | CTB [2→1] | SUM0 [5: 3], where JB [2→0] = $\overline{A_2}$ | $\overline{B_2}$ + $\overline{A_1}$ | $\overline{B_1}$ + $\overline{A_0}$ + $\overline{B_0}$, CTB [2→1] = ($\overline{A_2}$ + $\overline{B_2}$) | ($\overline{A_1}$ + $\overline{B_1}$) + $\overline{A_2}$ | $\overline{B_2}$, and SUM1 [5: 3] and SUM0 [5:3] are pairs of complementary sum bits.

Claim 23 (original): The adder of Claim 17, wherein each carry-create circuit has a stack height of two.

Claim 24 (original): The adder of Claim 17, wherein each carry-create circuit comprises:

first and second transistors connected in series between an output and a first node, the first transistor responsive to Ax, the second transistor responsive to Bx;

third and fourth transistors connected in series between the output and the first node, the third transistor responsive to Ay, the fourth transistor responsive to By; and

fifth and sixth transistors connected in series between the output and the first node, the fifth transistor responsive to Az, the sixth transistor responsive to Bz.

Claim 25 (original): The adder of Claim 17, wherein each carry-create circuit further comprises:

a PMOS pull-up transistor coupled between a supply voltage and the output, the pull-up transistor responsive to a clock signal; and

an NMOS pull-down transistor coupled between the first node and ground potential, the pull-down transistor responsive to a complement of the clock signal.

Claim 26 (original): The adder of Claim 17, wherein each carry-transmit circuit has a stack height of three.

Claim 27 (original): The adder of Claim 17, wherein each carry-transmit circuit comprises:

first and second transistors connected in parallel between an output and a first node, the first transistor responsive to Az, the second transistor responsive to Bz;

third and fourth transistors connected in series between the first node and a second node, the third transistor responsive to Ay, the fourth transistor responsive to By;

fifth and sixth transistors connected in parallel between the first node and a third node, the fifth transistor responsive to Ay, the sixth transistor responsive to By; and

seventh and eighth transistors connected in parallel between the third node and the second node, the sixth transistor responsive to Ax, the seventh transistor responsive to Bx.

Claim 28 (original): The adder of Claim 17, wherein each carry-transmit circuit further comprises:

a PMOS pull-up transistor coupled between a supply voltage and the output, the pull-up transistor responsive to a clock signal; and

an NMOS pull-down transistor coupled between the second node and ground potential, the pull-down transistor responsive to a complement of the clock signal.